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10/620,456	07/17/2003	Chin Lee	4444-0120P	9179

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EXAMINER	
CONTINO, PAUL F	
ART UNIT	**PAPER NUMBER**
2114	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary	Application No.	Applicant(s)	
	10/620,456	LEE, CHIN	
	Examiner	Art Unit	
	Paul Contino	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 10-17* is/are rejected.

7)☒ Claim(s) *9 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 March 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION: Final Rejection

Response to Arguments

1. Applicant's arguments with respect to claims 1-18 have been considered but are moot in view of the new grounds of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, 3, 4, 5, 7, 8, 10, 11, 12, 13, 15, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kiso et al. (U.S. Patent No. 5,757,809) in view of Wensley et al. (U.S. Patent No. 4,375,683).

As in claim 1, Kiso et al. teaches a memory modeling circuit with fault toleration, comprising:

a compare circuit, used to compare memory data stored in the same address in a plurality of memories *(Fig. 3, Pattern comparing circuit C; column 5 lines 41-43 and 46-53, which*

disclose the same address in a plurality of memories; and column 5 line 65 through column 6 line 3, which discloses a comparison of the data); and

a control circuit coupled to said plurality of memories, wherein said control circuit controls said memory data to be read or written from/to said plurality of memories *(Fig.3, the combination of Bin, Bout, J, and TM; columns 4-6)*.

However, Kiso et al. fails to teach of comparing at least three data inputs. Wensley et al. teaches of a compare circuit which compares at least three data inputs from different sources, wherein if the data inputs are divided into a first kind data and a second kind data and if the count of the first kind data outnumbers that of the second kind data, the compare circuit will output the first kind data *(Fig. 1; column 3 lines 65-67, column 4 lines 30-33 and 50-51, and column 7 lines 45-49)*.

It would have been obvious to a person skilled in the art at the time the invention was made to have included the multiple data comparison as taught by Wensley et al. in the invention of Kiso et al. This would have been obvious because the invention of Wensley et al. allows increases the fault tolerance of a computer system when memory data is being compared *(column 1 lines 49-68)*.

As in claim 2, Kiso et al. teaches a test circuit, receiving said memory data and the first kind data generated by said compare circuit to generate a testing result *(Fig. 3, the combination of Bout and J; column 6 lines 1-20)*.

As in claim 3, Kiso et al. teaches said test circuit further comprises a plurality of sub-test circuits with the same circuit design *(Fig. 4; column 5 lines 10-12, where the transistors of Bout are interpreted as sub-test circuits with a same circuit design).*

As in claim 4, Kiso et al. teaches said testing result gets an error code and then a faulty memory or a faulty sub-test circuit can be identified according to said error code *(column 6 lines 4-24, where the disagreement signal is interpreted as an error code).*

As in claim 5, Kiso et al. teaches said plurality of memories are the same type of memory *(column 4 lines 41-45, where it is interpreted that the memory cell arrays are of the same type of memory).*

As in claim 7, Kiso et al. teaches said compare circuit further comprises a plurality of sub-compare circuits with the same circuit design *(Fig. 2, AND gates; column 1 lines 42-43).*

As in claim 8, Kiso et al. teaches said control circuit is unable to receive the first kind data sent from said compare circuit while said control circuit is in the writing mode *(Fig. 3; column 5 line 44 through column 6 line 1, where it is interpreted that the transfer gates are open only during reads and writes, which occur at different times than one another – when data is being written, kind data will not be received because reception of kind data occurs during a read mode).*

As in claim 10, Kiso et al. teaches a memory modeling circuit with fault toleration, comprising:

a compare circuit, used to receive memory data stored in the same address in a plurality of memories and comparing the data with each other *(Fig. 3, Pattern comparing circuit C; column 5 lines 41-43 and 46-53, which disclose the same address in a plurality of memories; and column 5 line 65 through column 6 line 3, which discloses a comparison of the data)*;

a control circuit connecting said plurality of memories, wherein said control circuit enters a writing mode and writes information to the same address in said plurality of memories or enter a reading mode to load data from said compare circuit *(Fig.3, the combination of Bin, Bout, J, and TM; columns 4-6)*; and

a test circuit receiving the memory data stored in the same address in said plurality of memories and the first a kind data generated by said compare circuit to generate a testing result *(Fig. 3, the combination of Bout and J; column 6 lines 1-20)*.

However, Kiso et al. fails to teach of comparing at least three data inputs. Wensley et al. teaches of a compare circuit which compares at least three data inputs from different sources, wherein if the data inputs are divided into a first kind data and a second kind data and if the count of the first kind data outnumbers that of the second kind data, the compare circuit will output the first kind data *(Fig. 1; column 3 lines 65-67, column 4 lines 30-33 and 50-51, and column 7 lines 45-49)*.

It would have been obvious to a person skilled in the art at the time the invention was made to have included the multiple data comparison as taught by Wensley et al. in the invention of Kiso et al. This would have been obvious because the invention of Wensley et al. allows

increases the fault tolerance of a computer system when memory data is being compared *(column 1 lines 49-68)*.

As in claim 11, Kiso et al. teaches said test circuit further comprises a plurality of sub-test circuits with the same circuit design *(Fig. 4; column 5 lines 10-12, where the transistors of Bout are interpreted as sub-test circuits with a same circuit design)*.

As in claim 12, Kiso et al. teaches said testing result can identify a faulty memory or a faulty sub-test circuit *(column 6 lines 23-24)*.

As in claim 13, Kiso et al. teaches said compare circuit further comprises a plurality of sub-compare circuits with the same circuit design *(Fig. 2, AND gates; column 1 lines 42-43)*.

As in claim 15, Kiso et al. teaches said plurality of memories are the same type of memory *(column 4 lines 41-45, where it is interpreted that the memory cell arrays are of the same type of memory)*.

As in claim 17, Kiso et al. teaches said control circuit is unable to receive the first kind data sent from the compare circuit while said control circuit is in the writing mode *(Fig. 3; column 5 line 44 through column 6 line 1, where it is interpreted that the transfer gates are open only during reads and writes, which occur at different times than one another – when data is*

being written, kind data will not be received because reception of kind data occurs during a read mode).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 6 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kiso et al. in view of Wensley et al. (U.S. Patent No. 4,375,683) and in further view of Roohparvar (U.S. Patent No. 7,047,455).

As in claims 6 and 16, Kiso et al. teaches of RAM memory *(column 4 line 40)*. However, Kiso et al. fails to teach of SDRAM. Roohparvar teaches of SDRAM *(column 6 lines 61-65, where an SDRAM interface implies SDRAM)*.

It would have been obvious to a person skilled in the art at the time the invention was made to have included the SDRAM as taught by Roohparvar in the invention of Kiso et al. This would have been obvious because the invention of Roohparvar teaches of SDRAM, which allows for storing of information when power is off so as not to lose data *(column 1 lines 21-27)*, in a memory testing environment exhibiting fault tolerance.

* * *

4. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kiso et al. in view of Wensley et al. (U.S. Patent No. 4,375,683) and in further view of Ricchetti et al. (U.S. Patent No. 6,957,371).

As in claim 14, Kiso et al. teaches of an error code. However, Kiso et al. fails to teach of an engineer and repair. Ricchetti et al. teaches that a testing result gets an error code and then an engineer knows the fault part according to different error code combinations and repair said fault part to keep the reliability *(column 14 lines 43-49 and column 15 lines 32-33, where a user is interpreted as an engineer).*

It would have been obvious to a person skilled in the art at the time the invention was made to have included the engineer and repair as taught by Ricchetti et al. in the invention of Kiso et al. This would have been obvious because communicating fault information corresponding to a particular component to a user allows in order to repair a system, as taught by Ricchetti et al., increases the overall ability for a computer system to continue functioning properly and safely.

Allowable Subject Matter

5. Claims 9 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter:

Claims 9 and 18 disclose limitations involving data that may be received and data that may not be received by a control circuit. When read within the remainder of the limitations of the respective claims, claims 9 and 18 are allowable over the prior art.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

U.S. Patent 4,794,601 Kikuchi discloses comparing at least three data outputs.

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Contino whose telephone number is (571) 272-3657. The examiner can normally be reached on Monday-Friday 9:00 am - 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PFC
5/1/2007

SCOTT BADERMAN
SUPERVISORY PATENT EXAMINER